| Notice of Allowability | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/629,269 | ESKELDSON ET AL. | |
| | Examiner | Art Unit | |
| | Carol S Tsai | 2857 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--*

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *07/29/2003*.

2. ☒ The allowed claim(s) is/are *1-6*.

3. ☒ The drawings filed on *29 July 2003* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   **Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 11/12/2004
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

## DETAILED ACTION

## EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Edward L. Miller on December 15, 2004.

The application has been amended as follows:

IN THE ABSTRACT:

"A sampling transition-through-a-selected-voltage-detector sets two latches to different values when an input signal comparator referenced to the selected voltage transitions during a sample interval: at the beginning of the sample interval one latch receives one comparison value while at the end of the sample interval the other latch receives an opposite comparison value. A difference (XOR) in latched values for the transition detection latches indicates a transition through the selected voltage during the sample interval. A solution to the problem of such a transition-through-a-selected- voltage detection mechanism's insensitivity to steady state voltages may be solved by including an additional latch that is set by a second input signal comparator whose reference voltage is offset slightly from that used to detect transitions through the selected voltage, and that is also clocked at the start of the sample interval. Thus there are two latches clocked at the start of the sample interval. If they are different, as indicated by

another XOR, then the input was between the reference voltage and its slightly offset counterpart, even if the input signal was not in transition, or was steady state, at the start of the sample interval. The OR of the two XORs is the desired sampled indication of the value of the input signal for the sample interval, and is latched into an output latch, either at the start of the sample interval (for a pipelined system where the output is one state behind the samples) or is latched after delay no greater than the length of the sample interval (for a non-pipelined system)."

has been changed to

"A sampling transition-detector sets two latches to different values when an input signal comparator referenced to the selected voltage transitions during a sample interval: at the beginning one latch receives one comparison value while at the end the other latch receives an opposite comparison value. A difference (XOR) in latched values indicates a transition through the selected voltage during the sample interval. An additional latch is set by a second input signal comparator whose reference voltage is offset slightly from the selected voltage, It also clocked at the start of the sample interval. If the two latches clocked at the start of the sample interval are different, as indicated by another XOR, then the input was between the reference voltage and its offset counterpart. The OR of the two XORs is the desired indication."

***Allowable Subject Matter***

2. Claims 1-6 are allowed.

3. The following is an examiner's statement of reasons for allowance:

U.S. Patent No. 6,046,644 to Pitot et al. is the reference closest to the claimed invention. Pitot et al. disclose a phase-locked loop oscillator comprising: an oscillator circuit comprising two programmable-delay transition propagation circuits, based on cascades of logic gates with intermediate connectors and on multiplexers, with one data input, one setting input and one data output, looped by means of two D type logic flip-flop circuits with a data input D set at the logic level 1, a clock input CK, a zero-setting R input, a one-setting S input and a data output Q, each programmable-delay transition propagation circuit controlling, by its data output, the clock input CK of one of the D type logic flip-flop circuits and the zero-setting R input of the other D type logic flip-flop circuit, and each D type logic gate controlling, by its data output Q, the data input of the programmable-delay transition propagation circuit controlling its zero-setting R input and a two-input "AND" type logic gate interposed between the data output Q of one of the D type flip-flop circuits and the input of the programmable-delay circuit that is connected to it so as to constitute an inhibition command and oscillation activation input, two up/down counters based on combinations of logic circuits providing for the control of the setting inputs of the two programmable-delay transition propagation circuits, a divider circuit based on combinations of logic circuits connected, at the output of the oscillator circuit, to the data output Q of one of the D type logic flip-flop circuits, a phase comparator circuit based on combinations of logic circuits that receives, at input, the oscillator signal after division by the divider circuit and a phase reference signal, and detects the phase shift between these two signals, and a decision circuit, based on combinations of logic circuits, that is controlled by the phase comparator circuit and prepares the commands of the up/down counter circuits providing for the control of the setting inputs of the programmable-delay transition propagation circuits as a function of the state of

phase shift detected by the phase comparator circuit. However, Pitot et al. do not teach a method of measuring the level of a recurring data signal at selected times relative to a recurring reference associated with the data signal, the method comprising the steps of: (a) comparing the instantaneous voltage of a clock signal associated with the data signal to a clock threshold voltage to produce a logical clock signal; (b) delaying the logical clock signal by a selected first amount to produce a delayed logical clock signal; (c) comparing the instantaneous voltage of the data signal to be measured to a first data threshold voltage to produce a first logical data signal; (d) delaying the first logical data signal by a selected second amount to produce a first delayed logical data signal; (e) delaying the delayed logical clock signal by a selected third amount to produce a doubly delayed logical clock signal; (f) capturing the value of the first delayed logical data signal in response to the delayed logical clock signal; (g) capturing the value of the first delayed logical data signal in response to the doubly delayed logical clock signal; (h) generating the XOR of the value captured in step (f) and the value captured in step (g); comparing the instantaneous voltage of the data signal to be measured to a second data threshold voltage to produce a second logical data signal; (j) delaying the second logical data signal by the selected second amount to produce a second delayed logical data signal; (k) capturing the value of the second delayed logical data signal in response to the delayed logical clock signal; generating the XOR of the value captured in step (f) and the value captured in step (k); (m) generating the OR of the XOR values generated in steps (h) and (1); and (n) capturing the logical value of the OR operation generated in step (m), and including all of the other limitations in the independent claim.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Farrow discloses a method and apparatus for numerically controlling a ring oscillator.

Hunter discloses a circuit arrangement for measuring a time interval by evaluating the number of complete cycles, and/or the fraction of a cycle, of a ring oscillator that occur(s) during the time interval to be measured, in which there are provided means to avoid a count ambiguity if the time interval ends at or about the completion of a cycle of the ring oscillator.

Pinto et al. disclose a phase-locked loop circuit and method for producing an output signal which is phase locked with respect to an input signal.

Miyazawa discloses a phase locked loop circuit, which is arranged for receiving a first signal having a given frequency and producing a second signal which has the same frequency and is synchronous with the first signal, comprises control voltage generating means for generating a control voltage responding to a phase difference and a frequency difference between the first and second signals, a voltage controlled oscillator containing a ring oscillator having a multiplicity of the rows of inverters for producing a frequency output which is primarily

determined by the control voltage, and a quantity-of-rows changing means for automatically changing the quantity of the inverters rows in the ring oscillator according to the control voltage.

Bower discloses a circuit for providing an oscillatory driving signal from the point in time when power is supplied to a predetermined point in time thereafter.

Swanson et al. disclose a digital oscillator with output frequency accurately changeable from one period to the next.

***Contact Information***

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carol S. W. Tsai whose telephone number is (571) 272-2224. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (571) 272-2216. The fax number for TC 2800 is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC 2800 receptionist whose telephone number is (571) 272-1585 or (571) 272-2800.

In order to reduce pendency and avoid potential delays, Group 2800 is encouraging FAXing of responses to Office actions directly into the Group at (703) 872-9306. This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the

examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2800 will be promptly forwarded to the examiner.

Carol S. W. Tsai
Patent Examiner
Art Unit 2857

03/01/04